REMARKS/ARGUMENTS

The Applicants originally submitted Claims 1-22 in the application. In previous responses, the Applicants amended Claims 1, 8 and 15. In the present response, the Applicants have amended Claims 1, 5, 8, 12, 15 and 19. No claims have been cancelled or added. Accordingly, Claims 1-22 are currently pending in the application.

I. Rejection of Claims 1-4 and 8-11 under 35 U.S.C. §102

The Examiner rejected Claims 1-4 and 8-11 under 35 U.S.C. §102(b) as being unpatentable over U.S. Patent No. 5,528,513 to Vaitzblit, *et al.* ("Vaitzblit"). The Examiner asserts that Vaitzblit teaches each and every element of independent Claims 1 and 8. (Examiner's Action, page 2). The Applicants respectfully disagree.

Vaitzblit does not teach managing multitasking in a processor including acknowledging events based on code of a currently-active context. (Claims 1 and 8). Vaitzblit teaches a video file server having a scheduler that allows for performance guarantees for real-time streams to be maintained in the presence of randomly varying and unpredictable interactions and requests. (Column 3, lines 17-21). The scheduler determines whether a currently running task needs to be preempted whenever the real-time stream (an isochronous task) arrives at the server. Vaitzblit teaches to preempt the currently running task if the arriving task is an isochronous task and/or an isochronous task with a higher priority than the currently running task. (Column 4, lines 48-60).

Thus, Vaitzblit teaches preempting currently running tasks based on priority. As asserted by the Examiner, priority is a relative criticality between tasks. (Examiner's Action, page 6). Vaitzblit, therefore, teaches preempting based on a relationship between two tasks. More

specifically, Vaitzblit teaches preempting by comparing the criticality of one task to the criticality of another task and does not teach acknowledging events based on code of a currently-active context as recited in Claims 1 and 8. Consequently, Vaitzblit does not teach each and every element of the claimed invention associated with independent Claims 1 and 8 and Claims dependent thereon. Accordingly, the Applicants respectfully requests the Examiner to withdraw the §102(b) rejection with respect to Claims 1-4 and 8-11.

II. Rejection of Claims 5 and 12 under 35 U.S.C. §103

The Examiner rejected Claims 5 and 12 under 35 U.S.C. §103(a) as being unpatentable over Vaitzblit in view of U.S. Patent No. 6,009,454 to Dummermuth, *et al.* (Dummermuth). The Examiner has cited Dummermuth for teaching instruction counts. (Examiner's Action, pages 2-3). Dummermuth is directed to a multi-tasking operating system which is provided by recognizing that both ladder-type and state-type programs can be considered as simply a collection of individual instructions linked together by an implicit pointer list. (Column 2, lines 48-53).

As discussed above, however, Vaitzblit does not teach each and every element of independent Claims 1 and 8. Furthermore, Vaitzblit does not suggest each and every element of Claims 1 and 8 since Vaitzblit specifically teaches preempting based on priority. Dummermuth also does not teach or suggest managing multitasking in a processor including acknowledging events based on code of a currently-active context. (Claims 1 and 8). Instead, Dummermuth teaches executing programs according to a fixed number of allocated instructions. (Abstract). Dummermuth, therefore, fails to cure the deficiencies of Vaitzblit.

Since neither Vaitzblit nor Dummermuth, individually or in combination, teach or suggest each and every element of independent Claims 1 and 8, the combination of Vaitzblit and Dummermuth fails to establish a *prima facie* case of obviousness regarding dependent Claims 5 and 12 which includes the elements of Claims 1 and 8, respectively. Accordingly, the Applicants respectfully traverse the Examiner's rejection of Claims 5 and 12 under 35 U.S.C. §103(a) and request the Examiner withdraw the rejection with respect to these claims.

Furthermore, Dummermuth fails to teach or suggest activating contexts corresponding to background tasks based on instructions executed by each of the background tasks wherein each of the background tasks accomplishes an equal amount of work before a cycle of background processing repeats as recited in Claims 5 and 12. On the contrary, Dummermuth discloses a multi-tasking operating system for real-time control of industrial processes that controls the number of instructions in each task so that a given task may be ensured complete execution prior to task switching to coordinate between tasks. (Column 8, line 66 to Column 9, line 12). The number of instructions is a predetermined number that depends on the task and is selected to substantially complete the execution of the task. (Column 10, lines 8-14). The number of instructions executed for each task, therefore, vary depending on the task such that the tasks do not accomplish an equal amount of work before a cycle of background processing repeats as recited in dependent Claims 5 and 12.

III. Rejection of Claims 6 and 13 under 35 U.S.C. §103

The Examiner rejected Claims 6 and 13 under 35 U.S.C. §103(a) as being unpatentable over Vaitzblit in view of U.S. Patent No. 5,239,652 to Seibert, *et al.* ("Seibert"). As discussed above,

Vaitzblit does not teach or suggest each and every element of independent Claims 1 and 8. Furthermore, Seibert does not cure the deficiencies of Vaitzblit. Instead, Seibert is directed to reducing the power consumption of a computer by determining when the central processing unit is not actively processing and generating a power-off signal to a control logic circuit. (Abstract). Since neither Vaitzblit nor Seibert, individually or in combination, teach or suggest each and every element of independent Claims 1 and 8, the combination of Vaitzblit and Seibert fails to establish a *prima facie* case of obviousness of independent Claims 1 and 8 and dependent Claims 6 and 13 which include the elements of Claims 1 and 8, respectively. Accordingly, the Applicants respectfully traverse the Examiner's rejection of Claims 6 and 13 under 35 U.S.C. §103(a) and request the Examiner withdraw the rejection with respect to these claims.

IV. Rejection of Claims 7 and 14 under 35 U.S.C. §103

The Examiner rejected Claims 7 and 14 under 35 U.S.C. §103(a) as being unpatentable over Vaitzblit in view of U.S. Patent No. 6,256,659 to McLain, Jr. *et al.* As discussed above, Vaitzblit does not teach or suggest each and every element of independent Claims 1 and 8. Furthermore, McClain does not cure the deficiencies of Vaitzblit. Instead, McClain is directed to performing hybrid preemptive and cooperative multi-tasking by executing a number of logical units of work before interrupting a task. (Abstract). Since neither Vaitzblit nor McLain, individually or in combination, teach or suggest each and every element of independent Claims 1 and 8, the combination of Vaitzblit and McLain fails to establish a *prima facie* case of obviousness of independent Claims 1 and 8 and dependent Claims 7and 14 which include the elements of Claims 1 and 8, respectively. Accordingly, the Applicants respectfully traverse the Examiner's rejection

of Claims 7 and 14 under 35 U.S.C. §103(a) and request the Examiner withdraw the rejection with respect to these claims.

V. Rejection of Claims 15-18 and 22 under 35 U.S.C. §103

The Examiner rejected Claims 15-18 and 22 under 35 U.S.C. §103(a) as being unpatentable over Vaitzblit in view of U.S. Patent No. 5,713,038 to Motomura. As discussed above, Vaitzblit does not teach or suggest managing multitasking in a processor including acknowledging events based on code of a currently-active context as claimed in independent Claim 15. Furthermore, Motomura does not cure the deficiencies of Vaitzblit. Instead, Motomura is directed to a microprocessor that has a register file which allows a higher speed, more flexible, context switching as compared to conventional microprocessors. (Column 3, lines 15-17).

Since Vaitzblit does not teach each and every element of independent Claim 15 and Motomura does not cure its deficiencies, then the combination of Vaitzblit and Motomura does not establish a *prima facie* case of obviousness of independent Claim 15 and Claims dependent thereon. Accordingly, the Applicants respectfully traverse the Examiner's rejection of Claims 15-18 and 22 under 35 U.S.C. §103(a) and request the Examiner withdraw the rejection with respect to these claims.

VI. Rejection of Claims 19-21 under 35 U.S.C. §103

The Examiner rejected Claims 19-21 under 35 U.S.C. §103(a) as being unpatentable over Vaitzblit and in further view of Dummermuth, Motomura, Seibert, McClain or a combination thereof. As discussed above, Vaitzblit does not teach or suggest managing multitasking in a

processor including acknowledging events based on code of a currently-active context as claimed in independent Claim 15. Furthermore, Dummermuth, Motomura, Seibert, McClain or a combination thereof does not cure the deficiencies of Vaitzblit.

Since Vaitzblit does not teach each and every element of independent Claim 15 and Dummermuth, Motomura, Seibert, McClain or a combination thereof does not cure its deficiencies, then the Examiner can not establish a *prima facie* case of obviousness of independent Claims 19-21 which includes each and every element of Claim 15. Accordingly, the Applicants respectfully traverse the Examiner's rejection of Claims 19-21 under 35 U.S.C. §103(a) and request the Examiner withdraw the rejection with respect to these claims.

VII. Conclusion

In view of the foregoing remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-22. The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

HITT GAINES, P.C.

J. Joel Justiss
Registration No. 48,981

Dated: 8/8/03

P.O. Box 832570
Richardson, Texas 75083
(972) 480-8800
jjustiss@abstractassets.com